B.Tech IV Year I Semester
JNTUA COLLEGE OF ENGINEERING (AUTONOMOUS) PULIVENDULA
19AEE75b- DIGITAL SIGNAL PROCESSORS AND APPLICATIONS
(Open Elective-III)

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Course Objectives: The objectives of the course are to make the students learn about
- Provide the basic knowledge of different DSP Processors.
- Interfacing Memory and I/O Peripherals to different Programmable DSP Devices
- Operation of the ADC and programming modes
- Introduction to Field Programmable Gate Arrays
- Provide the basic knowledge of different DSP Processors.

UNIT – I: **10 Hrs**
Introduction to the TMSLF2407 DSP Controller: Brief Introduction to Peripherals - Types of Physical Memory - Software Tools
C2XX DSP CPU and instruction set: Introduction to the C2xx DSP Core and Code Generation - The Components of the C2xx DSP Core - Mapping External Devices to the C2xx Core and the Peripheral Interface -System Configuration Registers –Memory - Memory Addressing Modes - Assembly Programming Using the C2xx DSP Instruction Set
Learning Outcomes:
At the end of this unit, the student will be able to
- Able to understand the basic concepts of DSP controller   **L1**
- Able to understand the Assembly language programming   **L2**

UNIT – II: **10 Hrs**
Parallel and Serial Data Transfer: Pin Multiplexing (MUX) and General Purpose I/O Overview - Multiplexing and General Purpose I/O Control Registers - Using the General Purpose I/O Ports, Serial Communication
Learning Outcomes:
At the end of this unit, the student will be able to
- Understand the Pin Multiplexing and GPIO pins   **L1**
- Analyze the serial Communication concepts   **L2**
- Understand the concept of control Registers   **L3**

UNIT – III: **10 Hrs**
Interrupt system of TMS320LF2407: Introduction to Interrupts - Interrupt Hierarchy - Interrupt Control Registers - Initializing and Servicing Interrupts in Software, real time control with interrupts
The analog-to-digital converter (ADC): ADC Overview - Operation of the ADC and programming modes
Learning Outcomes:
At the end of this unit, the student will be able to
- Understand the concept of Interrupts   **L1**
- Analyze the concept of Analog to digital converter   **L2**

UNIT – IV: **10 Hrs**
Event Managers (EVA, EVB): Overview of the Event Manager (EV) - Event Manager Interrupts - General Purpose (GP) Timers- Compare Units - Capture Units and Quadrature Encoded Pulse (QEP) Circuitry - General Event Manager Information – PWM Signal Generation with Event Managers and interrupts, Measurement of speed with Capture Units, Implementation of Space Vector Modulation with DSP TMSLF2407A

Learning Outcomes:
At the end of this unit, the student will be able to
- Understand the concept of Event Manager and Interrupts   **L1**
- Apply the concept of Space Vector Modulation with processor   **L2**

UNIT – V: **10 Hrs**
Field Programmable Gate Arrays: Introduction to Field Programmable Gate Arrays – CPLD Vs FPGA – Types of FPGA , Configurable logic Blocks (CLB), Input/Output Block (IOB) – Programmable Interconnect Point (PIP)- HDL programming –overview of Spartan 6 & ISE Design Suite, Implementation of PWM technique with SPARTAN-6 FPGA

Learning Outcomes:
At the end of this unit, the student will be able to
- Understand the concept of Field Programmable Gate Arrays.   **L1**
- Apply the concept of HDL programming and PWM technique implementation   **L2**

Text Books:
1. Hamid A. Tolyat, "DSP based Electromechanical Motion Control"-CRC press, 2004
2. Wayne Wolf,,,FPGA based system design", Prentice hall, 2004

Reference Books:
1. Application Notes from the website of Texas Instruments
2. Spartan-6 FPGA Configurable Logic Block, 2010
3. Xilinx Spartan 6 Data sheets

Course Outcomes:
At the end of this Course the student will be able to
- Write Assembly Language Programs for the Digital Signal Processors   **L1**
- Configure and use Digital Input / Output lines and ADCs   **L2**
- Configure and use Interrupts and Event Managers for PWM generation   **L3**
- Employ DSPs &   **L4**
- FPGAs for the real time control of Power Electronic Controllers   **L5**